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Microwave Resistivity of Thermally Oxidized High Resistivity Silicon Wafers

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We used a microwave dielectric resonator to study how the process of thermal oxidation of high resistivity silicon wafers reduces the wafer microwave resistivity. Measurements were performed before surface thermal oxidation, after the oxidation, and after wet oxide removal. We show that the process of oxide growth decreases the microwave resistivity of the wafer from approximately 20 kΩ cm to as low as 400 Ω cm (typically to 1–2 kΩ cm), depending on the dielectric layer thickness and the growth process conditions. After the wet removal of SiO_2, the resistivity of the wafers increased, but it did not reach the initial value.

Key words: High resistivity silicon, microwave resistivity, thermal oxidation

High resistivity silicon (HRS, $\rho \geq 1$ kΩ cm) substrates are widely applied semiconductors in microwave and terahertz technology. HRS is used, e.g., as a base material for silicon monolithic microwave integrated circuits (Si MMICs) or, especially in recent years, as a convenient substrate for radio-frequency devices,[1–3] including those that are emerging and based on novel low-dimensional materials, such as ultrafast graphene photodetectors[4] or graphene coplanar waveguides (CPW).[5] The advantages of using HRS wafers are their easy accessibility, relatively low price, and low level of high-frequency dissipation losses, which are important factors for operating RF devices and for propagating the microwave signal. The main disadvantage of using HRS substrates is a bias-dependent leakage current effect, which could lead to unintentional shortening of the designed circuitry through the poorly conducting substrate. To remove this obstacle, the surface of the HRS wafer can be oxidized to produce a dielectric layer. Unfortunately, the process of oxide growth can significantly reduce the sheet resistance of the wafer, as shown by Reyes,[6] Wu,[7] and Gamble.[8] Examining the problem of microwave signal losses in CPW fabricated on high resistivity silicon substrates, they found that the microwave signal losses increased from approximately 2 dB/cm up to 18 dB/cm at 30 GHz[7,8] when the surface of HRS was covered with the silicon dioxide dielectric layer. This result was an important finding because such high dissipation losses could make MMICs on SiO_2/HRS substrates useless, despite the significant reduction in the leakage currents. The increased dissipation was explained by the emergence of surface states that trap the inversion/accumulation charges and prevent them from going to the conduction/valence band, thereby lowering the effective surface resistivity of the Si covered with SiO_2. Solutions that have been considered, so far, when attempting to solve the problem of excessively low sheet resistance include selective etching of the SiO_2 layer or deposition of a polycrystalline silicon buffer layer between the Si and the SiO_2.

In this paper, we bring important evidence on the influence of the SiO_2 thermal growth process on the HRS resistivity. We show that the process significantly lowers the microwave resistivity of the HRS wafer and that the value of the resistivity is not reversible after the oxide removal. In order to show

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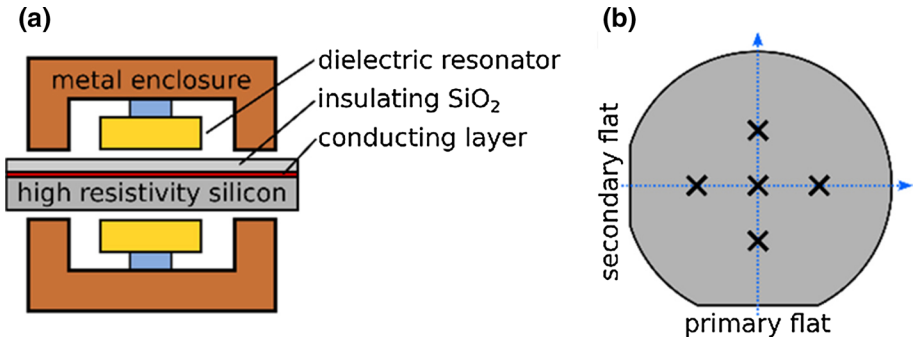

Fig. 1. (a) Schematic of the experimental setup (split-post microwave resonator operating at 4.5 GHz), (b) the locations on the silicon wafer where point measurements were performed ("x" symbol). Blue dotted lines indicate the scan directions (Color figure online).

this, we used the microwave cavity technique[9] as a research tool because it has the following properties: (1) it is a contactless technique that does not require a fabrication process, (2) it allows wafer mapping, (3) it allows measurements at different stages of the silicon wafer production process, and (4) it allows probing of the resistivity of a conducting layer sandwiched between two insulating/poorly conducting layers, which is not possible in the case, e.g., of the four-point probe method. Measurements were performed before surface oxidation, after the oxidation, and after oxide removal to determine whether the emergence of a conducting layer at the Si/SiO_2 interface is the only reason for the resistivity decrease and to what extent the wafer resistivity can be restored.

High resistivity silicon wafers (diameter 4″, thickness 525 μm, orientation 100, boron doping, resistivity ≥10 kΩ cm, one side polished) were produced by Topsil Semiconductor Materials S.A. via the flat zone method. The resistivities of pristine wafers were determined using a microwave split-post resonator operating at approximately 4.5 GHz[9] just before the process of oxide growth. In order to exclude place-dependent results, the measurements were performed at five points on the wafer (see Fig. 1). We emphasize that no significant differences among these points were observed, and the averaged results, which confirm the information given by the producer, are presented in Table I.

Next, silicon wafers were oxidized in a Thermco horizontal furnace. Prior to the oxidation process, the wafers were cleaned in RCA standard solutions. Three different oxidation process recipes were used to obtain high-quality silicon oxide layers of a required thickness within a reasonable period of time:

- *Recipe 1* (gives SiO_2 layer with thickness of 10 nm): (1) heating up to 950°C in N_2/O_2 (20:1); (2) temperature stabilization in N_2; (3) oxidation in N_2/O_2 (3.3:1); (4) N_2 purge; (5) cooling down to 800°C in N_2.
- *Recipe 2* (gives SiO_2 layer with thickness of 20–100 nm): (1) heating up to 950°C in N_2/O_2 (20:1); (2) temperature stabilization and pre-oxidation in N_2/O_2 (3.3:1); (3) oxidation in dry O_2; (4) N_2 purge; (5) cooling down to 800°C in N_2.
- *Recipe 3* (gives SiO_2 layer with thickness of 300 nm): (1) heating up to 950°C in N_2/O_2 (20:1); (2) temperature stabilization and pre-oxidation N_2/O_2 (3.3:1); (3) oxidation in dry O_2; (4) oxidation in $O_2 + H_2$, (5) oxidation in dry O_2; (6) N_2 purge; (7) cooling down to 800°C in N_2.

The oxide thickness was measured using spectroscopic ellipsometry, which is the most common and widely used approach to determine the precise value of the oxide layer.[10,11] The error in estimation of the oxide thickness is approximately 1 nm. Modeling of an $air/SiO_2/Si$ structure was used to calculate the thickness of the layer, assuming a Cauchy model for the optical properties of the oxide.

Immediately after the thermal oxidation process, the resistivities of the wafers were determined again using the microwave resonator. The values of the resistivities measured at the center of the wafer are presented in Table I. The following comments should be made regarding the data.

First, it can be clearly seen that after thermal oxidation of HRS wafers, their resistivities significantly decreased (averaged drop in resistivity equals 94%). This observation is consistent with previously published reports[6–8] because the wafer resistivity is directly related to the microwave losses. This can be explained using the definition of the complex relative permittivity, which can be written using following equation:

$$\varepsilon_r = \varepsilon_r' - j\varepsilon_r'' - j\frac{\sigma}{\omega\varepsilon_0}$$

where ε_0 is the permittivity of vacuum, ε_r is the relative complex permittivity, ε_r' is the real part of the relative complex permittivity, ε_r'' is the imaginary part of the relative complex permittivity, ω is the angular frequency, and σ is the material conductivity. From the formula above it can be seen that the imaginary term includes both dielectric losses and losses related to the conductivity.

Table I. Values for the resistivity of the HRS wafers before oxide growth, after oxide growth, and after oxide removal

HRS wafer number	1	2	3	4	5	6	7	8	9	10
Oxide thickness (nm)	10[a]	20[b]	28[b]	38[b]	50[b]	50[b]	50[b]	75[b]	103[b]	302[c]
ρ_1—resistivity before oxide growth (Ω cm)	23147	22646	21803	22188	21649	24439	22705	23471	24057	21105
ρ_2—resistivity after oxide growth (Ω cm)	1401.6 −93.9%	617.41 −97.3%	1057.9 −95.1%	1046.1 −95.3%	962.51 −95.5%	1023 −95.8%	1134.6 −95.0%	855.81 −96.3%	2246.8 −90.7%	2641.4 −87.5%
ρ_3—resistivity after oxide removal (Ω cm)	15100 −34.8%	7820 −65.5%	10900 −50.0%	9930 −55.2%	5770 −73.3%	–	–	4120 −82.4%	4910 −79.6%	4770 −77.4%
ρ_3/ρ_2	10.8	12.7	10.3	9.49	5.99	–	–	4.81	2.18	1.81

The percentage resistivity drop is calculated with respect to the initial resistivity value.[a]recipe 1.[b]recipe 2.[c]recipe 3.

Second, in order to properly interpret the results one needs to remember that in the case of a homogenous material, resistivity is a property of this material. However, in the case of the HRS wafer covered with SiO_2, one can distinguish at least four layers within the wafer: bulk silicon layer, depletion layer, inversion layer, and dielectric layer. Thus, obtained results of the resistivity need to be treated as the total resistivity of all parallel layers, and its value is dominated by the most conducting layer. For further discussion, please see Ref. 12.

Finally, in contrast to the measurements on pristine wafers, we observed significant differences in the resistivity value that depends on the place on the wafer. Therefore, we constructed a microwave resistivity line scanner based on a microwave split-post dielectric resonator operating at approximately 14 GHz. Higher resonant frequency implies that the resonator has a reduced active area (change in active area diameter from approximately 15 mm down to 3 mm), which allows scanning at a step size of 2 mm. For each sample, two scans crossing at the center of the wafer were performed—one parallel and one perpendicular to the primary flat (see Fig. 1). The results of the microwave resistivity scans are shown in Fig. 2. The increases in resistivity at the boundaries have no physical meaning and are related to the evacuation of the sample from the active area of the resonator. Significant resistivity variations were observed over the samples. For the 10-nm thick SiO_2 sample, the resistivity increased from an average value of approximately 1.6 kΩ cm to approximately 2.0 kΩ cm in the center of the wafer. For the 20-nm thick SiO_2 sample, the resistivity value changed from approximately 400 Ω cm to approximately 1.2 kΩ cm. For the 28-nm thick SiO_2 sample, the resistivity was almost constant, with no distinct features, in contrast to the sample with the 38-nm thick SiO_2 layer, for which a resistivity peak in the center of the wafer can be observed. For the 50-nm thick SiO_2 sample, the resistivity changed from approximately 900 Ω cm to approximately 1.2 kΩ cm, whereas for the 75-nm thick SiO_2 sample, the change was from approximately 700 Ω cm to approximately 1 kΩ cm. For samples with the thickest dielectric layers of 103 nm and 302 nm, the resistivity changed from a relatively high value of approximately 2 kΩ cm to much greater than 5 kΩ cm.

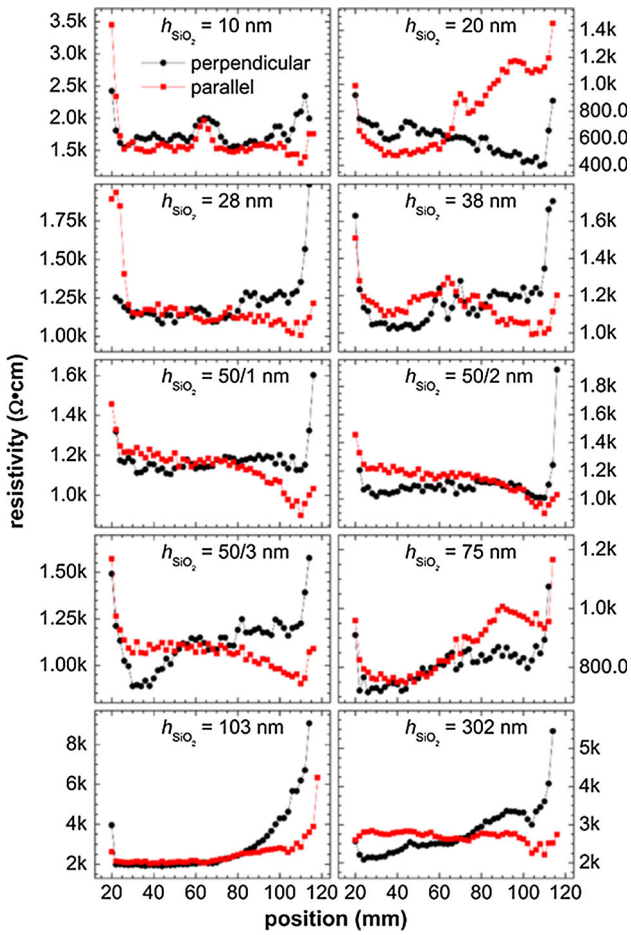

Fig. 2. Resistivity scans of the HRS wafers covered by SiO_2 dielectric layers of different thicknesses. The perpendicular (black plot) and parallel (red plot) directions are fixed with respect to the primary flat. The increase in resistivity at the boundary has no physical meaning and is related to the evacuation of the sample from the active area of the resonator (Color figure online).

According to some works,[6–8] the decrease in the resistivity results in the emergence of surface states that trap the inversion/accumulation charges and prevent them from going to the conduction/valence band, thereby lowering the effective surface resistivity of the Si covered with SiO_2. Based on this explanation we expect that in our case the observed variation of the resistivity stems from the variations in interface properties, such as charge trap density or the width of the interface, which according to Queirolo[13] depends on oxide thickness.

Next, we verify whether the resistivity of the wafers can be restored upon oxide removal. Thus, just after a complete series of measurements on oxidized samples, silicon dioxide was removed using a very selective etching process performed in BHF (buffered hydrofluoric acid solution). The resistivities of the restored wafers were determined using the microwave split-post resonator at five points (see Fig. 1) and no significant differences were observed among them (similar to the results of the measurements before oxidation and in contrast to the measurements after oxidation). The averaged results are presented in Table I. The resistivity values are significantly lower than the initial ones, particularly for the thickest oxide layers. We also note that the ρ_3/ρ_2 ratio, that illustrates the increase in resistivity due to oxide removal, decreases with increasing oxide thickness. Two possible explanations for the resistivity decrease are: (1) irreversible decrease in the bulk silicon resistivity after high temperature treatment and/or (2) existence of new or preserved surface states after oxide removal. The former one is related to the time of the wafer stay at elevated temperatures, which is higher for thicker oxides, and thus wafers with thicker oxide are longer exposed to potentially harmful conditions. The latter one is related to the width of the interface which is increasing with increasing oxide thickness. Because at the interface the amount of oxygen changes continuously, the BHF etching, which removes oxide, but not silicon might have left some part of the interface meaning rarely distributed oxide atoms in the silicon matrix. Such remains could constitute new or preserved states that are efficient microwave energy dissipation centers. However, more detailed analysis requires further studies (e.g. EELS spectroscopy or SIMS spectrometry), which will allow distinguishing the contribution from surface states and bulk properties.

In summary, we have shown in a straightforward manner that thermal oxidation of the HRS wafer is not a trivial process and can lead to a significant decrease in the mean resistivity. We attribute the resistivity decrease mainly to the emergence of the conductive layer on the Si/SiO_2 interface. We demonstrate that the conductivity of this layer is inhomogeneous and that oxide removal using buffered hydrofluoric acid solution does not restore the resistivity to its initial value. Our findings could be useful for the semiconductor industry because we demonstrate how to perform fast and robust evaluation of the influence of the oxide growth process on an HRS wafer. These findings could also be useful for designers of RF circuitries on the very popular HRS/SiO_2 substrates and for those in the scientific community who are interested in the physical properties of Si/SiO_2 interfaces.

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